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EXAMINER	
NALVEN, ANDREW L	
ART UNIT	**PAPER NUMBER**
2134	

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08/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,852	PAATERO, LAURI	
	Examiner	Art Unit	
	Andrew L. Nalven	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4-14 are pending.

Response to Arguments

2. Applicant's arguments filed 7/9/2007 have been fully considered but they are not persuasive.

3. Applicant has argued on pages 7-8 that Grohoski and Aaro fail to teach a device with a secure and normal mode with modes indicated by a configuration register and which register is set by a processor in the device. Examiner respectfully disagrees. Grohoski teaches a cryptographic accelerator (Grohoski, paragraph 0056, paragraph 0106, crypto processor) and teaches a configuration register that is set by a processor (Grohoski, paragraph 0061, CPU stores data in the control queue). Grohoski does not specifically disclose dual modes of operation. However, as noted in the prior office action, Aaro also teaches a configuration register arranged to indicate to the accelerator whether secure mode or normal mode is set by the processor arranged in the device device (Aaro, column 4 lines 55-61, column 3 lines 30-67, column 3 lines 4-30). Aaro teaches an embodiment whereby a user may interface with software and use the keypad and display in instructing the device to enter secure mode (Aaro, column 3 lines 4-30). Because the user is interfacing with software the user is also interfacing with the processor in instructing a move to secure mode. As a result, the processor will

command the unit to enter secure mode. Thus, Examiner maintains that the combination of Grohoski and Aaro teach all of the limitations of the instant claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-2, 4-9, 11-14 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Grohoski et al US PGPub 2004/0225885 in view of Aaro et al US Patent No. 6,662,020

5. **With regards to claims 1, 11-12, 14**, Grohoski teaches an electronic device comprising (Grohoski, paragraph 0056, paragraph 0106, crypto processor), an accelerator for accelerating cryptographic data processing operations, which acceleration is arranged with (Grohoski, paragraph 0056, higher speed encryption and decryption processes enabled using crypto coprocessor) a first logical interface over which data to be processed is provided (Grohoski, paragraphs 0061-0062, transfers crypto packet), a secure second logical interface over which cryptographic keys employed in the operation of processing data is provided (Grohoski, paragraph 0062, paragraph 0052, control queue, paragraphs 0056-0057, sharing access to registers and memory access units provides a secure connection, paragraph 0106, controlled access

to secure registers), and wherein the first logical interface and the secure second logical interface share a same physical interface (Grohoski, paragraph 0056, share same memory access units). Grohoski fails to teach a configuration register arranged to indicate to the accelerator whether secure mode or normal mode is set by the processor arranged in the device. However, Aaro teaches a configuration register arranged to indicate to the accelerator whether secure mode or normal mode is set by the processor arranged in the device (Aaro, column 4 lines 55-61, column 3 lines 30-67, column 3 lines 4-30, menus are accessed by user to allow setting of mode). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Aaro's method of providing secure operation modes for a processor because it offers the advantage of helping provide safe and secure sensitive transactions by providing an increased level of security (Aaro, column 1 lines 51-57).

6. **With regards to claim 4**, Grohoski as modified teaches the configuration register is further arranged such that is may be set in one of a plurality of possible encryption modes, the accelerator being arranged to operate in the encryption mode set in the register (Grohoski, paragraph 0116, encryption type field).

7. **With regards to claim 5**, Grohoski teaches the accelerator is arranged such that the first logical interface and the secure second logical interface are provided via respective physical interfaces (Grohoski, Figure 2 Items 215 and 210).

8. **With regards to claim 6**, Grohoski fails to teach the first logical interface of the accelerator is arranged such that it is accessible by any application while the secure second logical interface of the accelerator is arranged such that it is accessible by

protected applications only. However, Aaro teaches the first logical interface of the accelerator is arranged such that it is accessible by any application while the secure second logical interface of the accelerator is arranged such that it is accessible by protected applications only (Aaro, column 4 lines 55-61, only secure applications can access secure memory with keys, column 4 lines 23-40, all applications can access encryption using WAP or GPRS). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Aaro's method of securing an interface because it offers the advantage of helping provide safe and secure sensitive transactions by providing an increased level of security (Aaro, column 1 lines 51-57).

9. **With regards to claim 7**, Grohoski as modified teaches protected applications prevent other applications from accessing the accelerator (Grohoski, paragraph 0106).

10. **With regards to claim 8**, Grohoski as modified teaches protected applications are applications which are allowed to execute in the secure execution environment (Aaro, column 4 lines 55-61).

11. **With regards to claim 9**, Grohoski teaches storage circuitry arranged with at least one storage area in which protected data relating to device security is located (Grohoski, paragraph 0106). Grohoski fails to teach a processor with separate operating modes and different memory access restrictions. However, Aaro teaches a processor arranged such that is may be set in one of at least two separate operating modes (Aaro, column 4 lines 55-61, column 3 lines 30-67) and the device further arranged such that the processor is given access to said storage area when a normal

processor operating mode is set (Aaro, column 4 lines 55-61) and the processor is denied access to said storage area when a normal processor operating mode is set (Aaro, column 4 lines 55-61) and the processor is capable of accessing the secure second logical interface of the accelerator when the secure processor operating mode is set (Aaro, column 4 lines 55-61, only secure applications can access secure memory with keys, column 4 lines 23-40, all applications can access encryption using WAP or GPRS). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Aaro's method of securing an interface because it offers the advantage of helping provide safe and secure sensitive transactions by providing an increased level of security (Aaro, column 1 lines 51-57).

12. **With regards to claims 13**, Grohoski teaches the acceleration arranged such that the first logical interface and the secure second logical interface share a same physical interface (Grohoski, paragraphs 0102-0103, access using the interface include both keys and source data, paragraph 0056, share same memory access units).

13. **Claim 10 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Grohoski et al US PGPub 2004/0225885 and Aaro et al US Patent No. 6,662,020, as applied to claim 9 above, and in further view of Srinivasan et al US PGPub 2004/0158742.

14. **With regards to claim 10**, Grohoski as modified fails to teach the protected applications controlling the processor operation mode. However, Srinivasan teaches the protected applications controlling the processor operation mode (Srinivasan,

paragraph 0010). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Srinivasan's method of setting secure mode because it offers the advantage of helping allow an application to enforce authorization requirements and rights requirements for restricted content (Srinivasan, paragraph 0007).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew L. Nalven whose telephone number is 571 272 3839. The examiner can normally be reached on Monday - Thursday 8-6, Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 571 272 3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Nalven

KAMBIZ ZAND
SUPERVISORY PATENT EXAMINER